ALLOWED CLAIMS

1. A semiconductor integrated circuit device comprising:

a logic circuit including a plurality of areas, each of the areas including at least a first MOS transistor of a first conductivity type;

a substrate bias control circuit to control a state of the logic circuit, an output impedance to drive a substrate bias voltage of the first MOS transistor in a first state being lower than the output impedance to drive the substrate bias voltage of the first MOS transistor in a second state;

first and second power supply lines to supply the logic circuit with the supply voltage;

a first substrate bias voltage supply line; and

a plurality of second MOS transistors of the first conductivity type, at least one of the second MOS transistors being provided to the plural areas;

wherein the control circuit controls the logic circuit to be in the first state when a supply voltage of the logic circuit is activated,

wherein a source of the first MOS transistors is connected to the first power supply line, a drain of the first MOS transistor is connected to the second power supply line and the substrate bias voltage of the first MOS transistor is supplied via the first substrate bias voltage supply line,

wherein a source-drain path of each of the second MOS transistors are provided between the first power supply line and the first substrate bias voltage supply line, and

wherein the plurality of the second MOS transistors are controlled to be ON state when the logic circuit is in the first state.

2. The semiconductor integrated circuit device according to claim 1,

wherein the substrate bias control circuit includes a power-on resetting circuit to generate a reset signal in accordance with the supply voltage of the logic circuit, and

wherein the control circuit controls the logic circuit to be in the first state in response to the reset signal.

3. The semiconductor integrated circuit device according to claim 1,

wherein when the logic circuit is in the first state, an absolute value of a threshold voltage of the first MOS transistor is a first value by controlling the substrate voltage, and

wherein when the logic circuit is in the second state, the absolute value of the threshold voltage of the first MOS transistor is a second value higher than the first value by controlling the substrate voltage.

5. The semiconductor integrated circuit device according to claim 1, further comprising:

a second substrate bias voltage supply line;

a plurality of fourth MOS transistors of a second conductivity type, at least one of the fourth MOS transistors being provided to the plural areas;

wherein each of the areas includes at least a third MOS transistor of the second conductivity type,

wherein a source of the third MOS transistor is connected to the second power supply line, a drain of the third MOS transistor is connected to the first power supply line and the substrate bias voltage of the third MOS transistor is supplied via the second substrate bias voltage supply line;

wherein a source-drain path of each of the fourth MOS transistor is provided between the second power supply line and the second substrate bias voltage supply line; and

wherein the plurality of the fourth MOS transistors are controlled to be ON state when the logic circuit is in the first state.

6. The semiconductor integrated circuit device according to claim 1, further comprising:

a first substrate bias voltage generator to generate a first voltage;

wherein when the logic circuit is in the second state, the plurality of the second MOS transistors are controlled to be OFF state and the first voltage is supplied to the first MOS transistors via the first substrate bias voltage supply line from the first substrate bias voltage generator.

7. The semiconductor integrated circuit device according to claim 5, further comprising:

a second substrate bias voltage generator to generate a second voltage;

wherein when the logic circuit is in the second state, the plurality of the fourth MOS transistors are controlled to be OFF state and the second voltage is supplied to the third MOS transistors via the second substrate bias voltage supply line from the second substrate bias voltage generator.